IFW

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VIRGINIA 22313-1450 ON:
Date of Deposit: **October 28 2004**
Name of Person Making Deposit: **Nicole Barrese**
Signature: Nicole Barrese 10/28/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: **Haining Yang, et al.**	Date: **October 28, 2004**
Serial Number: **10/711,897**	Examiner:
Filed: **October 12, 2004**	Confirmation No: Group Art Unit:
Title: **METHOD AND STRUCTURE FOR IMPROVING CMOS DEVICE RELIABILITY USING COMBINATIONS OF INSULATING MATERIALS**	IBM Corporation D/18G, B/300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 CFR 1.56, and further pursuant to 37 CFR 1.97 and 37 CFR 1.98, Applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

Pursuant to 37 CFR 1.97 (b) (3), no fee is believed to be necessary.

Respectfully submitted,
Haining Yang, et al.

By: James J. Cioffi
James J. Cioffi, Attorney
Registration No. 51,564
Tel. (845)894-3363

Enclosure

INFORMATION DISCLOSURE CITATION

(Use Several sheets if necessary)

ATTY DOCKET NO.	APPLICATION NO.
FIS920040194US1	10/711,897
YANG ET AL.	
FILING: 10-12-04	GROUP ART

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		1	T. G. Gerence et al., "The Combined Effects of Deuterium Anneals and Deureated Barrier-Nitride Processing on Hot-Electron Degradation in MOSFET's;" IEEE Transactions of Electron Devices, Vol. 46, No. 4, April 1999; pages 747 - 753.
		2	J. H Stathis; "Reliability limits for the gate insulator in CMOS technology;" IBM J. Res & Dev. Vol. 46 No. 2/3 March/May 2002; pages 265 - 286.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		3	T. H. Ning; "Why BiCMOS and SOI BiCMOS?;" IBM J. Res & Dev. Vol. 46 No. 2/3 March/May 2002; pages 181 - 186..

EXAMINER	DATE CONSIDERED

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